SIEMENS

DESIGO™ PX OPEN
PX RS-Bus
Engineering guide

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Building Technologies

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1 About this document

1.1 Revision history

Version	Date	Changes	Chapter/Section	Pages
_00	16.11.2007	Field test version		

1.2 Before you start

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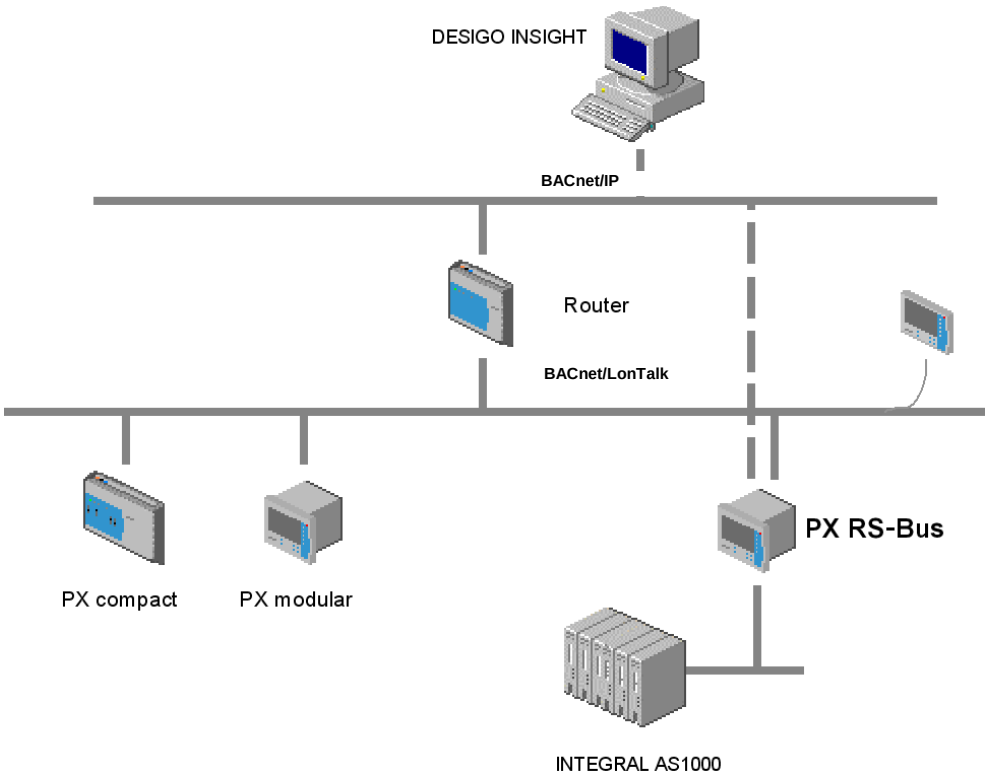
2 Introduction

The PX RS solution is based on the PXC00-U + PXA30-RS hardware (PXC64-U or PXC128-U are also admissible). The solution allows the integration of INTEGRAL AS1000 automation stations [NRU, NRK etc] directly into the DESIGO PX automation level. This document provides an overview for engineering, installing and commissioning the PX RS solution.
Details regarding AS1000 and the DESIGO system are not covered.

3 System overview

3.1 Topology

The diagram below details the system topology connections for PX RS together with the AS1000 subsystem and DESIGO.



3.2 Glossary

DESIGO PX OPEN	Offers fort he integration of third-party systems and devices.
PX RS-Bus	Solution name.
PXC00-U	Modular hardware for integration solutions.
PXA30-RS	Extension module inside PXC00-U for communications towards the field level.
PXC-RS	"Device" that must be selected in DTS / XWORKS for the integration.

3.3 Features overview

PX RS operates as a valid member of the RS bus, conforming to the rules and regulations of operation similar to a NICO-N Interface.

- The PX RS interface is used to read and write to data point registers in AS1000 modules.
- Data point registers in the AS1000 modules are mapped to BACnet objects in the PX RS interface.
- DESIGO reference mapping strings are used for the PX RS relation to the AS1000 data point register.
- The PX RS is connected directly to the RS bus using the RS485 port or via a NARC using the RS232 port.

3.4 Supported AS1000data point registers

- All standard physical data point registers: UI, DI, UO, DO.
- All setpoint, calculated and parameter data points: UZ, DZ, UP, DP, US, DS.
- InterRS data point registers: UA, DA, UE, UE.
- Time clock register: DU.
- Alarm registers: DX, DY, DR.
- Operating mode and mode registers: OM and DW.
- Runtime totalizers: RTT.
- Module status: RSS.
- Time synchronization: TS

- Supported number :
  - INTEGRAL max. 1000 DP
  - DESIGO max. 2000 DP
    (certain INTEGRAL DPs are mapped to more than one DESIGO DP).

3.5 Extended features and functions

The PX RS solution also allows for a number of enhanced features:

- Time synchronization of the RS bus is supported.
- InterRS operation enhanced by using pseudo RS addressing when needed.
- PX RS can operate on the RS bus alongside existing NICO-N/Nitel interfaces.

4 Engineering overview

As other PX OPEN solutions, PX RS-Bus could be engineered manually. But in the case of PX RS-Bus the comfortable support of the 321 Workbench tool is available (see workflow description CM110776).

4.1 Mapping string

The mapping string is used in the engineering procedure to define the mapping of the AS1000 data point registers to BACnet objects.

Example: M = RSNr(RegType.RegNr[DataFormat])

RSNr:	1..16	RS module number
RegType:	See table	Register type number
RegNr:	See table	Register number
DataFormat:	BOOL for binary and FLOAT for analog data points	

For an index of the register type numbers, refer to the mapping table on page 22.

Important; Reading register values
The mapping rule above is valid where the interface is to read the data point register value in an RS module.

Important; Writing and reading values to/from a single register
Due to the design characteristics of DESIGO it is not possible to directly read back the value of an output object from the subsystem. Instead, the value must be read back as an input. This would present an addressing problem, as for two points having the same mapping information (string), only one data point is generated in the internal PX RS-Bus database. Therefore, the mapping information for an RS data point, that can be integrated both as input (read) and output (write), requires that two objects be created: an input with the standard mapping address, and an output with a mapping address offset of +100 added to the output register number. Refer to the UO/DO data point section for more details. The read back value can also be mapped as a feedback I/O.

Important; Writing and reading values from a single register and setting to Auto/Hand
Together with the above rules, certain output data points such as UO, UDO and DO can be set to Auto and Manual [hand]. In this situation, another set of values can be read and modified, requiring an additional offset to the mapped register. For more details, refer to the output engineering section.

4.2 Communication and message block

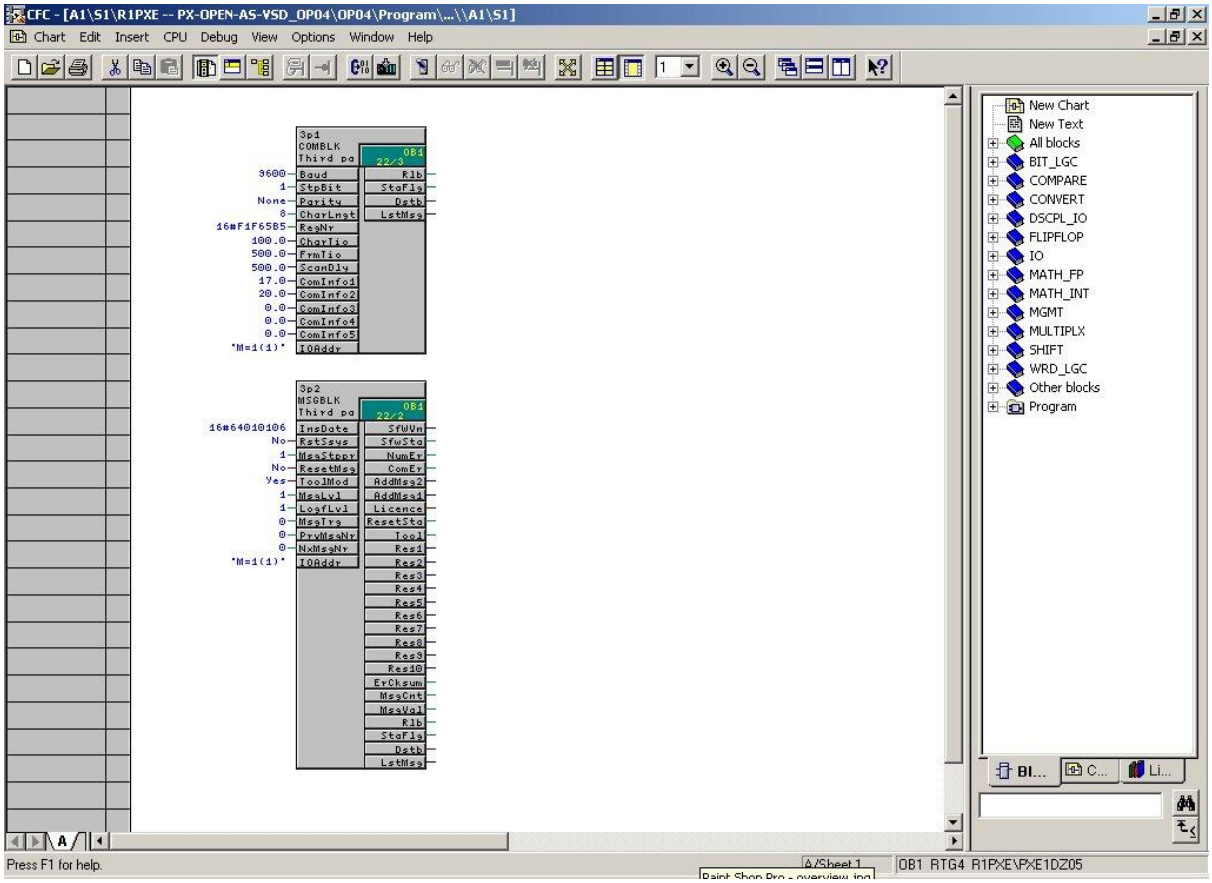
The communication and message discipline IO blocks must always be included in the PX RS-Bus structure. All pins except the following can be kept as default from the FW library:

Communication block pin	Value range	Description
RegNum	UINT32	Enter the license key
ComInfo1	1..32	PXE-RS address on the RS bus. If no value is entered 17 is used.
ComInfo2	30..100 ms	Application layer request delay [*1] If no value is entered 30ms is used.
IOAddr	M=1(1) fixed	I/O address (only internal use)

[*1] Delay between each application request to the RS bus. This delay reduces the load on the RS bus, allowing more time for other tasks in PX RS-Bus e.g. DMAP, BACnet etc. The data link layer has no delay.

Important: If the settings in the communication block are changed, the PX RS-Bus must be restarted (e.g. warm start from DTS) as these settings are only checked at startup (e.g. ComInfo1, PX RS-Bus address, ComInfo2 delay etc.)

Message block pin	Value range	Description
IOAddr	M=1(1) fixed	I/O address (only internal use)



4.3 Licensing and activating the solution

For ordering, licensing and download information, please consult your local sales office.

Activate the solution

For each automation station the license key must be entered in the Communication block in CFC (pin **RegNr**).

The message Block returns the following information:

Pin	**Inforation**
License	License accepted or not
Res1	License band: 0 = light, 1 = regular, 2 = full
Res2	Number of licensed points
Res3	Number of unused licensed points

4.4 Hierarchy

During the workflow with the 321 Workbench tool, the SAPIM engineering information is mapped to BACnet objects.

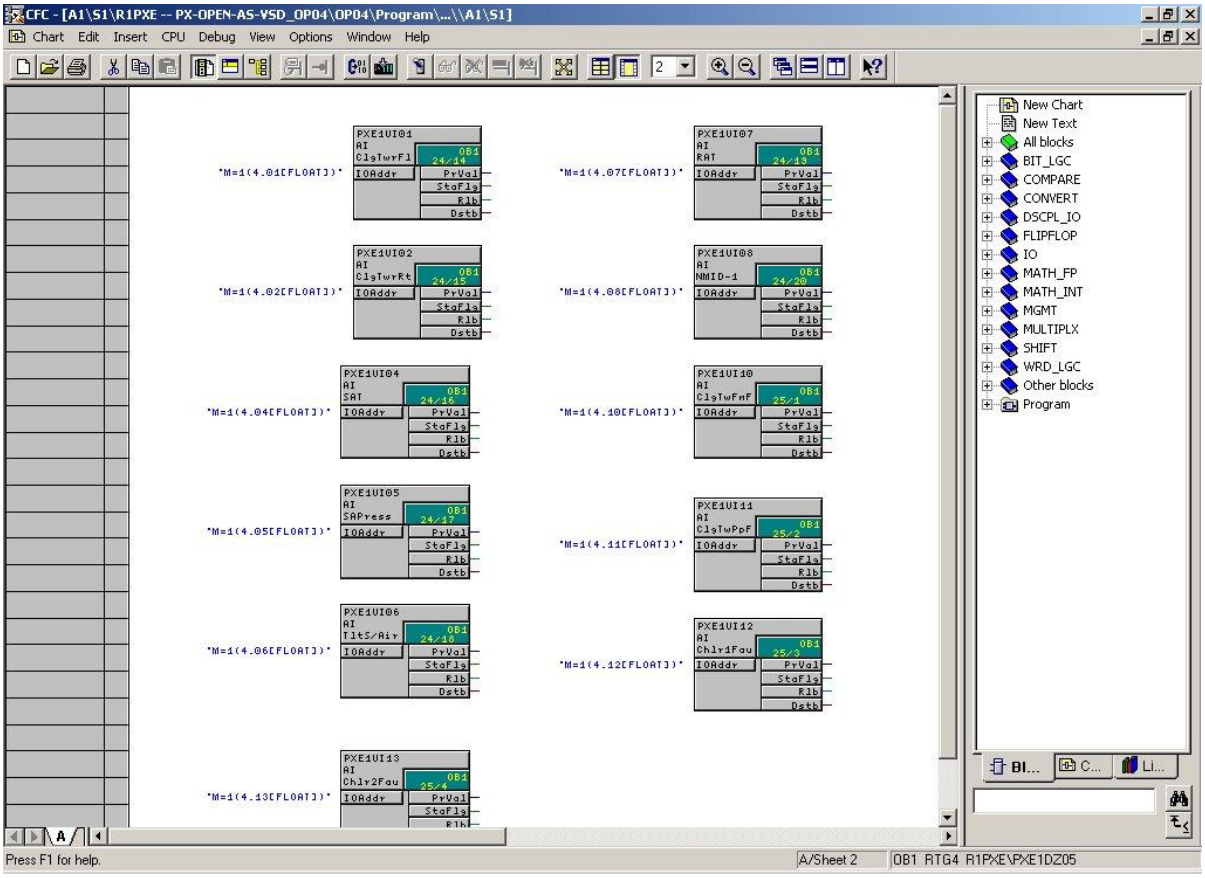
To represent the registers as BACnet objects in a useful manner, hierarchy information can and should be added. This allows the PXM20 and such to present the objects in a more readable and accessible form.

The hierarchy must be created manually.

5 Engineering details

5.1 UI, DI – Inputs

The physical input points are mapped to analog and digital I/O blocks. The diagram below is an extract from CFC editor showing the RS universal inputs mapped to analog input blocks.



M = RSNr(RegType.RegNr[DataFormat])

RSNr:	1..16	RS module number
RegType:	See table	Register type number
RegNr:	See table	Register number
DataFormat:	BOOL for binary and FLOAT for analog data points	

Example:	Integrate from RS module address 5, analog input UI 12.
AI input:	M = 5(4.12[FLOAT])

Important : Default slope and intercept are created by default when a PXE-RS is assigned in System Design of DESIGO TOOLSET. **These values must not be changed**. Check the polarity settings.

5.2 UZ, DZ - Calculated registers

Calculated registers are similar to physical inputs, as they are read-only.

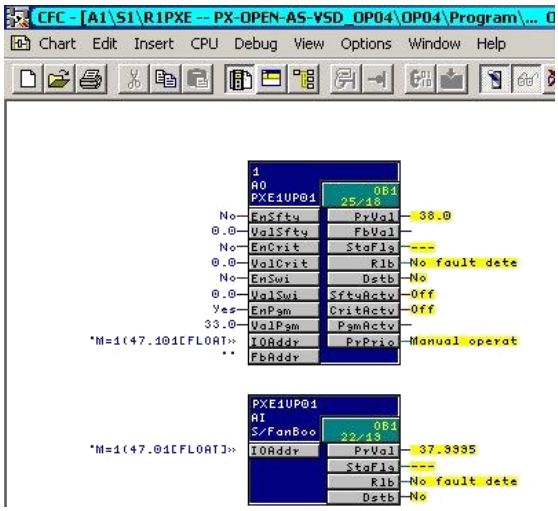
M = RSNr(RegType.RegNr[DataFormat])

Example: Integrate from RS module address 5, analog calculated UZ 12.
AI input: M = 5(50.12[FLOAT])

Important : Default slope and intercept are created by default when a PXE-RS is assigned in System Design of DESIGO TOOLSET. **These values must not be changed**. Check the polarity settings.

5.3 UP, DP – Parameters

Digital and analog parameters are mapped to analog and binary blocks. The diagram below shows an analog input block and an analog output block. Typically, the input can be mapped to the feedback I/O pin, FbAddr on the output block.



Important: These data points can be mapped as analog and binary outputs if DESIGO is required to write to these values. In such a case, addressing must adhere to the following rules:

Example: Integrate from RS module 5, UP 12 as input and output.
AI input: M = 5(47.**12**[FLOAT])
AO output: M = 5(47.**112**[FLOAT])

The input can be mapped to the feedback I/O pin, FbAddr of the output block if required.

Important: Default slope and intercept are created by default when a PXE-RS is assigned in System Design of DESIGO TOOLSET. **These values must not be changed**. Check the polarity settings.

5.4 US, DS – Setpoints

Digital and analog setpoints are similar to the parameters shown in the previous section. They can be read and written. US registers are mapped to analog objects and DS are mapped to binary objects.

Important: These data points can be mapped as analog and binary outputs if DESIGO is required to write to these values. In such a case, addressing must adhere to the following rules:

Example: Integrate from RS module 5, US 12 as input and output.
AI input: M = 5(44.**12**[FLOAT])
AO output: M = 5(44.**112**[FLOAT])

The Input can be mapped to the feedback I/O pin of the output object if required.

Important : Default slope and intercept are created by default when a PXE-RS is assigned in System Design of DESIGO TOOLSET.
These values must not be changed. Check the polarity settings.

5.5 UE, DE, UA, DA – InterRS register handling

In this solution, the registers are read and mapped to BACnet directly from the module as part of the normal scanning.

UE	Analog Input	
DE	Binary Input	
UA	Analog Input	PXE reading only
DA	Binary Output	PXE reading only

The InterRS data points can be read by PX RS-Bus by mapping these points to DESIGO I/O binary or analog I/Os with the I/O addresses set accordingly.

Example: Integrate from RS module 8, UA 3
Analog input AI: M = 8(16.3[FLOAT])

PX RS-Bus can also send out a UA value. The sender address must be 1..16, but not necessarily the PXE-RS's own address. This is a unique feature that can be used where existing modules are being replaced.

Example The PXE-RS has own address 17,
but must send out from address 3, DA 6
Binary output BO: M = 3(17.106[BOOL])

When PX-RS-Bus sends out an UA value the definition range is always fixed to 1 (-500..+500).

5.6 RSS – RS module status

The RSS RS module status contains information on the SAPIM structure of the RS module. When integrated, this point can also be used to check communication to the RS module, as the status for the corresponding I/O indicates if there is a communication failure.

The value for the RS module status is:

0 = RS module no SAPIM structure
1..15 = Counter increments every time a new SAPIM structure is loaded

A communication failure to the RS module is indicated with the Reliability pin (Rlb) of the corresponding DESIGO I/O block.

Communication OK:	Reliability = No Fault
Communication failure:	Reliability = Unreliable Object

To reduce the number of alarms from PX RS-Bus, the RSS are the only data points that are supervised for communication failure. The communication checks are done every minute Reliability changes to unreliable object for the specific RS module are done if a communication failure exists and an alarm can be sent out.

5.7 MODE – Operating mode

The operating mode shows which mode is active 1..16 (auto or manual).
The register number is not used internally in PX RS-Bus. but must be set to 1.

Example AI: M=6(42.1[FLOAT])

5.8 DW – Mode parameters

The DW shows a Boolean value to represent each of the possible mode states

Example: BI: M=6(57.1[BOOL])

5.9 DU – Time clock register handling

The time schedules stored in the AS1000 modules are directly accessed. Instead, the output register DU from the time clock is read and, if required, written to from the PX RS-Bus .

Example Write BO: M=6(19.101[BOOL])

Example Read BO: M=6(19.1[BOOL])

Note:
To prevent conflicting commands if the PX RS-Bus writes to the register, the local time schedules must either be deleted or disabled.

5.10 UO, OU OVR, DO, DO OVR - Output register handling

If two points have the same mapping information, only one data point is generated in the internal PX RS-Bus database. Therefore, the mapping information for an RS point that can be integrated both as input (read) and output (write) must have an offset +100 added to the output register number.

When PX RS-Bus writes an output to a RS module, the status for the data point in the RS module is set to Manual. If the RS data point must be set back to Auto, an additional data point must be integrated with an offset +1000 added to the register number. When a value <>0 for analog and on for digital is written, the RS data point is set back to auto.

Input Register:	1..99
Register no for Outputs:	101..199 (Manual, +100 offset)
Register no for Outputs:	1001..1099 (Auto, +1000 offset)

Example:	Integrate from RS module 7, UO3 as input.
AI input:	M = 5(7.**3**[FLOAT])

In the RS modules; there are two different registers for the DO and UO outputs: One showing the internal auto state (DO and UO); and one for manual override that also can be read (DO-OVR and UO-OVR).

Example:	Write to RS module 7, Output UO3 as Manual and Auto:
AO output (manual):	M= 7(10.**103**[FLOAT]
AO output (auto):	M= 7(10.**1003**[FLOAT]) (sets to auto when value<>0 is written)

For all I/Os, the I/O address string must be entered according to the syntax and scheme described earlier. For the DESIGO analog I/Os, the slope and intercept must be set to 1 and 0 respectively.

It would be possible for PX RS-Bus to set the status flag for an I/O block to Overridden to indicate that the corresponding RS data point was in manual operation vs. auto (status can only be OK, Overridden, Resolving or Invalid Handle). The problem then would be that a DESIGO BACnet client, e.g. PXM20 or INSIGHT, can not overwrite the I/O again as the Override status according to the

DESIGO system concept indicates that the local switch on the I/O module was set to override position. No other clients can write to the I/O unless the switch is reset to auto. This situation results in a deadlock with the I/O remaining in Override status which can never again be changed.

To allow a DESIGO user to reset an RS data point from Manual to Auto, an additional data point must be integrated with offset +1000 in the register number (manual write uses +100). When a value <>0 for analog and On for digital is written, the status changes to Auto.

Example: Write to RS module 7, Output UO3 as Manual and Auto:

AO output (manual): M= 7(10.**103**[FLOAT]
AO output (auto): M= 7(10.**1003**[FLOAT]) (sets to auto when value<>0 is written)

Example: Write to RS module 3, Output DO6 as Manual and Auto:

DO output (manual): M= 3(11.**106**[BOOL]
DO output (auto): M= 3(11.**1006**[BOOL]) (sets to auto when value = ON is written)

If only manual writing is required, the auto output is not required.

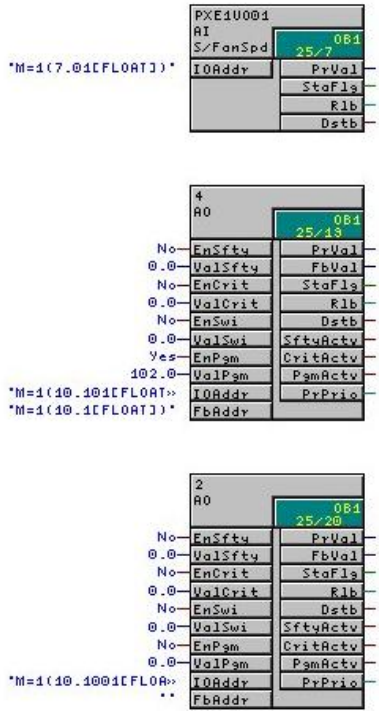
Important: When a release from manual is done for a BACnet point, the value returns to its default, program or other value depending on the logic for the I/O, and the new value is transmitted (DESIGO concept). Blocks in the CFC normally have their default and program values set to 0. To avoid 0 being written to the object after a release, the block's default/program value must be configured with a suitable value so as not to unexpectedly disrupt plant operation.

The diagram below is an excerpt from the CFC editor and details a possible configuration for an analog output.

The top object is an analog input used to read the actual value of the universal output. The next block, an output object, is used to write the Override value to the AS1000 output. It also has a feedback I/O pin address to show the value of the override at the AS1000 level (it may be different if the value is adjusted locally, for example with an NBRN).

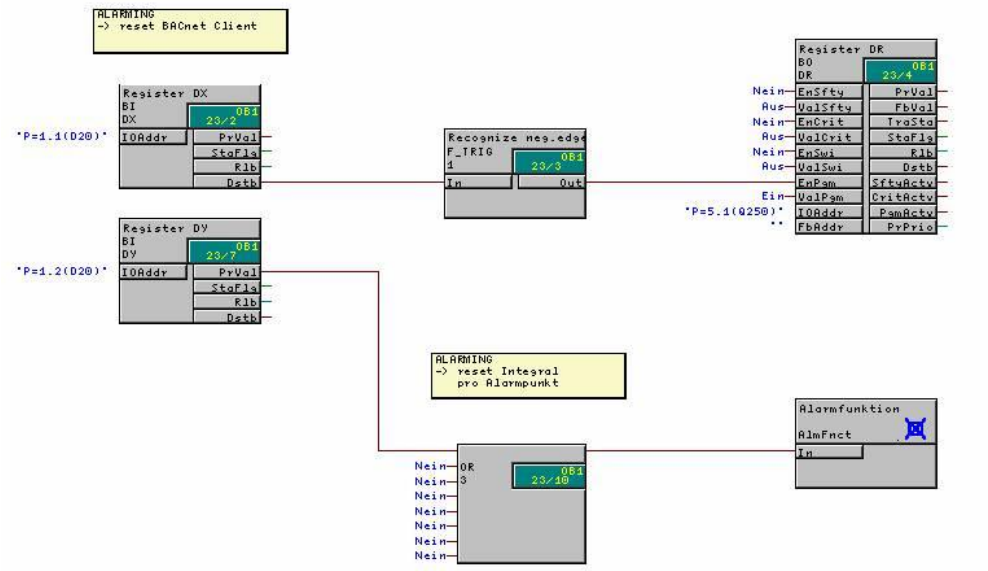
The last block is the Auto/Manual reset.

All these blocks can be incorporated into a compound to simplify use and engineering.



5.11 DX, DY, DR - Alarm handling

The following is a proposition how you can realize the alarming in CFC.
This proposition supports integrated alarming and alarm acknowledging on the INTEGRAL side as well as on the DESIGO side. The update on the operator units (DESIGO and INTEGRAL) will also be correct.



Function

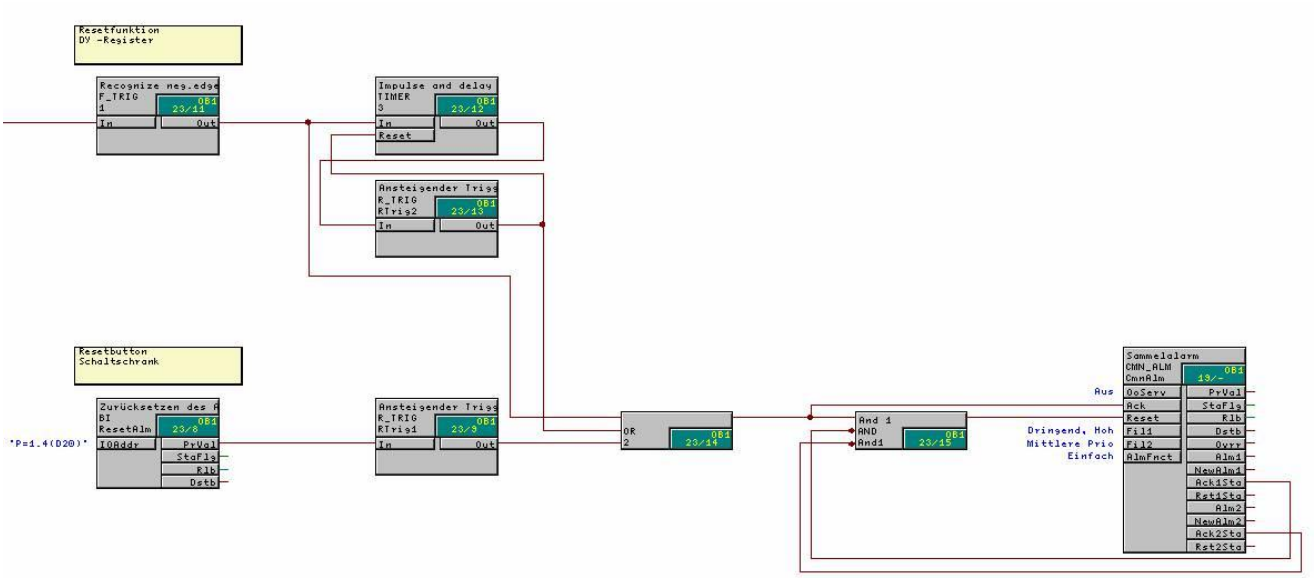
- The three upper compounds serve for indicating in DESIGO and for updating in INTEGRAL.
- The lower compounds serve for acknowledging in INTEGRAL and for updating in DESIGO.
- If there are several alarm emitting objects in INTEGRAL, their Register DY blocks can all be connected to the lower OR block.
  Each alarm emitting object requires the four blocks Register DX, Recognize neg. edge, Register DR and register DY.

Notes

- Replace the P bus addresses of the example with integration addresses (M = ...).
- When interconnected in the OR block, all no longer pending alarms (return from alarm, reverting to normal) for the INTEGRAL controller will be acknowledged (analogous to the reset key in the panel).

Compound "Alarm function"

- The Compound "Alarm function" (bottom right) is the CAS solution, amended with the upper three blocks.
- The reset button on the cabinet may not exist in your project.



6 Commissioning

6.1 Startup

Prerequisites

- PXC, PXA30-RS and RS bus installed and connected.
- Supply switched on.
- FW loaded.
- CFC application loaded with DTS.
- After loading you are asked if you wish to start PX.
  → start PX.

At startup. all input data points are read from the RS bus including their definition ranges. This is necessary to enable the data points to be converted correctly to and from the RS bus (the two value bytes are converted based on their definition range). During normal operation, the data points are read without their definition range, resulting in shorter telegrams and better performance.
In addition, all output data points that need to include a definition range for their values are read during startup to ensure that they are sent correctly when written later to the RS bus. The outputs are not written to the RS bus after a reset of PX RS-Bus to prevent overwriting problems with the AS1000 system. Only when output values are changed or retriggered are they sent to the RS bus.

6.2 PX RS-Bus as a valid member on the bus

PX RS-Bus is a valid bus member and occupies one address on the bus.

Engineering hint:
Although PX RS-Bus can coexist on the RS bus with a NICO interface, performance limitations inherent in PX RS-Bus may cause delays in responding to master assignment queries from the NICO. The resultant bus disturbance cause the NICO to reset intermittently.
Experience from the field shows that these resets can be practically eliminated by reengineering the database as follows:
In the INTEGRAL subsystem, register points can be designated as management points for viewing at the management station. If these same data points are mapped in PX RS-Bus, we recommend to remove the management point designation.

6.3 Read registers

To correctly handle the registers, the PX RS-Bus reads the scaling register on first scan.

6.4 Write registers

As with normal operation, output BACnet objects that have a different feedback value are written down. For more information on writing outputs, see 5.10.

6.5 Synchronize network system time

If time synchronizing of the AS1000 system is required, a MsgBlock is used to pass the correct format and command to the RS bus.
A time synchronization signal containing the current date and time can be sent from PX RS-Bus to all the RS modules.
Every time the digital output is changed (e.g. On/Off or Off/On), a time synchronization signal is sent with the current date and time of PX RS-Bus. As this is a broadcast message, PX RS-Bus in turn sends out a group address instead of a specific RS module address. However, in the I/O address mapping string, RS module number 1 and register number 101 must be put in although they are not used internally in PX RS-Bus.
This is done by including a binary output I/O with the following IO address:

Example: M=1(254.101[BOOL])

6.6 Resend same values

The DESIGO I/Os are normally configured with Switch_Kind = Normal, which means that only changed values are sent. If the I/O is configured as Switch_Kind=Trigger, it is not possible to resend the same value e.g. for a BO resend ON, or for an AO resend 26.4.

6.7 Digital data point polarity

Some digital data points defined in SAPIM are reversed. To allow for this, BACnet objects must have their polarity reversed to show the same state.

6.8 Priority scanning algorithm

The PX RS-Bus scans the engineered registers using a method similar to the NICO implementation. The table below details the point types and their weighting.

The RS data points are scanned according to the following priorities similar to the NICO Interface:

Scanning priority	Weight factor	RS data points
1	1	DY1, DY2, RSS
2	2	UI, DI, UZ, DZ
3	3	UO, DO, DU, DW
4	5	UE, UA, DE, DA
5	9	RTT, US, UP, DS, DP

The weight factor indicates how frequent a point is read within a complete read cycle of all points, e.g. a DY1 is read 3 times more often than a UO, and 9 times as often as a RTT.

6.9 Electrical transmission

The COM1 port can use RS485 for direct access to the RS bus or RS232 for access via a NARC.

COM1 / RS485	+ ------- RS1 - ------- RS2	NARC / NARB
COM1 / RS232	--- Null modem cable --- (2 and 3 crossed)	NARC

Communication settings

Communication settings fixed to
- 9600 baud
- 1 start bit
- 8 data bits
- No parity
- 1 stop bit

One address/data control bit (master sends address byte with bit=1 for multidrop wakeup mode, all other bytes with bit=0.
Slaves always send all bytes with bit=0).

7 Data point register mapping table

Register	Description	Register type	Register number	Read write	DESIGO I/O type	DESIGO data format	Comments
UI	Universal input	4	1..16	R	AI	FLOAT	
DI	Digital In input put	5	1..8	R	BI	BOOL	
UZ	Universal calculated	50	1..99	R	AI	FLOAT	
DZ	Digital calculated	51	1..99	R	BI	BOOL	
UO	Universal output	7	1..16	R	AI or AO feedback *3	FLOAT	Read output
UO OVR	Universal output override	10	1..16	R	AI or AO feedback *3	FLOAT	Read manual override (*1)
			101..116	W	AO	FLOAT	Write manual override (*1)
			1001..1016	W	AO	FLOAT	Set to Auto (*1)
DO	Digital output	8	1..8	R	BI	BOOL	Read output
DO OVR	Digital output override	11	1..8	R	BI	BOOL	Read manual override (*1)
			101..108	W	BO	BOOL	Write manual override (*1)
			1001..1008	W	BO	BOOL	Set to Auto (*1)
UP	Universal parameter	47	1..99	R	AI or AO feedback*3	FLOAT	
			101..199	W	AO	FLOAT	
DP	Digital parameter	48	1..99	R	BI	BOOL	
			101..199	W	BO	BOOL	
US	Universal setpoint	44	1..99	R	AI or AO Feedback*3	FLOAT	
			101..199	W	AO	FLOAT	
DS	Digital setpoint	45	1..99	R	BI	BOOL	
			101..199	W	BO	BOOL	
DY1	Common alarm 1	53	1..7	R	BI	BOOL	Alarm set DX 11..17
			11..17	R	BI	BOOL	Alarm memory DY 11..17
			101..107	W	BO	BOOL	Alarm reset DR 11..17

Register	Description	Register type	Register number	Read write	DESIGO I/O type	DESIGO data format	Comments
DY2	Common alarm 2	54	1..7	R	BI	BOOL	Alarm set DX 21..27
			11..17	R	BI	BOOL	Alarm memory DY 21..27
			101..107	W	BO	BOOL	Alarm reset DR 21..27
UE	Universal input InterRS	13	1..99	R	AI	FLOAT	
DE	Digital input InterRS	14	1..99	R	BI	BOOL	
UA	Universal output InterRS	16	1..99	R	AI	FLOAT	
			101..199	W	AO	FLOAT	PX RS-Bus send (*2)
DA	Universal output InterRS	17	1..99	R	BI	BOOL	
			101..199	W	BO	BOOL	PX RS-Bus send (*2)
OM	Operating mode	42	1	R	AI	FLOAT	
DW	Operation mode register	57	1..16	R	BI	BOOL	
DU	Clock Channel	19	1..8	R	BI	BOOL	Clock channel corresponds to register number
			101..108	W	BO	BOOL	Clock channel corresponds to register number
RSS	Module status	255	1	R	AI	FLOAT	
RTT	Runtime totalized	56	1..99	R	AI	FLOAT	
TS	Time synchronization	254	101	W	BO	BOOL	Send current date and time from PX RS-Bus (*4)

Notes

(*1) The RS modules contain two different registers for the DO and UO outputs: One shows the internal auto state (DO and UO) and one the manual override that also can be read (DO-OVR and UO-OVR).

(*2) PX RS-Bus can send out a UA value. The sender address must be 1..16 and not necessary the PXE-RS's own address.

(*3) Use of feedback is only allowed for analog points (DESIGO: Binary feedback is mapped to multistate which would cause problems).

(*4) Every time the digital output is changed (e.g. On/Off or Off/On), a time synchronization signal is sent with the current date and time of PX RS-Bus. As this is a broadcast message, PX RS-Bus sends out a group address instead of a specific RS module address. However, in the I/O address mapping string, a RS module number 1, and register number 1 must be put in although they are not used internally in PX RS-Bus.

Example: M=1(1.1 [BOOL])

8 Tips and tricks

8.1 System hierarchy in DTS

To optimize the DESIGO operations and attain the best performance for the PX RS it is important to utilize the hierarchy definitions and split the relevant data points into compounds. The PX RS tool can facilitate the creation of the DTS import file.

8.2 Mapping string

The mapping string is key to successful operation of the solution. If the integration appears to behave strangely, check the data point mapping strings. If these appear correct and you still have problems, reduce the data points, try working with only the physical inputs mapped first and then build up a database with additional data points.

8.3 Slope and intercept of object

When a PXE-RS is assigned, the correct slope and intercept values are given. These should not be changed so that the slope/intercept parameters in the RS module are correctly used.

8.4 PX RS-Bus connected to bus on startup

It is important to have the PX RS-Bus connected to the RS bus on startup. Due to the optimized communications, the PX RS-Bus reads the scaling of all integrated data points during the initial bus scan. This ensures correct decoding of all the various point types.

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